REMARKS

Drawings

The crosshatching pattern of the dielectric substrate and the through hole filler material as amended in Figure 4 are believed to comply with the "section of synthetic resin or plastic" symbol pursuant to MPEP 608.02, and that this symbol is most appropriate for these elements. Further along these lines, it is not believed that the alternating thick and thin lines of the substrate must share the same relative slope as those of the filler material. Upon indication by the examiner that informal Figure 4 is acceptable, all of the remaining figures will be amended accordingly and prepared as formal drawings.

Claim rejections – 35 USC § 103

Claims 9, 22 and 25. Claims 9, 22 and 25 are rejected under 35 USC § 103(a) as being unpatentable over Reed (U.S. Patent No. 4,964,948).

The law is quite clear that, in order for a claimed invention to be rejected on obviousness, the prior art must suggest the modifications sought to be patented; In re Gordon, 221 U.S.P.Q. 1125, 1127 (CAFC 1984); ACS Hospital System, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (CAFC 1984).

Reed does not teach the structure claimed in amended claim 9. As reflected in amended claim 9, an important advantage of the present invention is the **unetched** first circuitry line **additively plated** directly onto the through hole and **thereby electrically connected** to said plated through hole, the first circuitry line having a line width **equal to or less than** the plated through hole first diameter.

> The subtractive etch method of circuitization, described above, yields a subcomposite having limited wiring density. When conductive metal is etched to form spaces between lines of circuitry, the conductive metal which is covered by photoresist during formation of circuitry, is susceptible to erosion by the etchant in areas beneath the photoresist. To avoid this problem, the thickness of the circuit lines divided by the width of the spaces between them, i.e. the aspect ratio, must be sufficiently low to produce a functional product. The width of spaces limits wiring density. For example, a typical circuit board that has circuit lines about 1 mil thick, requires line and space widths of at least about 3 mils. Also, sharp edge definition, such as the formation of squared lines, is difficult to achieve using the subtractive etch method.

(See the specification at page 2, line 22, through page 3, line 5).

Arguing that mere routine experimentation was involved overlooks the second sentence of 35 USC 103. In re Saether (CCPA 1974) 492 F2d 849, 181 USPQ 36. The issue is whether the experimentation is within the teachings of the prior art. In re Waymouth et al. (CCPA 1974) 499 F2d 1273, 182 USPQ 290. Reed does not teaching the structure of amended claim 9, because Reed's teachings are limited to printed wiring board structures formed through subtractive etching processes. In order to address the problems clearly described in applicant's specification as provided above, namely the susceptibility of conductive metal covered by photoresist to erosion during the formation of circuitry by subtractive etching, Reed covers his through hole structure by a large layer of photoresist 46 significantly larger than his through hole, necessarily creating a conductive circuitry structure on top of his through hole significantly larger than the through hole.

> After the board 14 has been thoroughly dried, the resist 46 is applied on the conductive sheets 16 and 18 and over the tops of the hole plugs 44, *as is shown in FIG. 12*. The resist can be applied in any acceptable manner including the technique described in the previously mentioned U.S. Pat. No. 4,720,798..... The resist layer over the hole plugs is of *sufficient thickness to adequately protect the copper at the corners of the plated through-hole during the etching process*.
>
> After the resist 46 has been cured, the board is dipped into an etchant bath and *areas of the conductive sheets 16 and 18 which are not protected by the resist 46 are etched away*, to leave the pattern of circuit conductors on the exterior surfaces of the substrate 20.

Reed at column 8, line 52, through column 9, line 5 (emphasis added), and his Figure 12. As clearly illustrated by Figure 12, this resulting circuit area is much larger than his through hole. Reed further states that this larger surrounding area can be used to effect electrical connections to his through holes: "Solder would be applied only on the *outer surface* of the conductors *surrounding* the conductor." (Reed at column 9, lines 20-22).

Thus, Reed does not teach the structure claimed in amended claim 9, and the structure of amended claim 9 is not within his teachings. Reed unambiguously *requires* that his un-illustrated "conductor" be larger than and surround his through hole, in order to assure protection to the through hole during the etching process, and thus *cannot* teach the first circuitry line as claimed in amended claim 9.

Additionally, amended claim 9 teaches that the additively plated unetched first circuitry has a top surface and a bottom surface with a common width. This is possible due to the fact that the first circuitry is *additively plated* rather than *subtractively etched*. As described in

applicants' specification as provided above, subtractive etching results in undercutting of conductive metal areas below the resist areas. Therefore, subtractively etched circuit lines necessarily have an undercut type of structure, wherein the width of the bottom surface is necessarily less than the width of the top surface. In contrast, the present invention enables the formation of "square" circuit lines, as comprehended by the language of amended claim 9. This type of structure is not possible within the teachings of Reed, nor within any other prior art reference that teaches the formation of circuit lines through subtractive etching. Thus, *both* the (1) "additively plated" and (2) "unetched" limitations are outside the scope of the teachings of Reed.

Therefore, amended claim 9 is believed allowable over Reed. Claims 22 and 25 are dependent upon, and include all of the limitations of amended claim 9, and are for the same reasons believed to be allowable over Reed.

New independent claim 28 has been added. The subject matter of new claim 28 is believed to be allowable over Reed for the same reasons established above. Reed cannot be modified to teach an *additively plated unetched metal pad* having a bottom surface plated directly onto the at least one plated through hole and thereby electrically connected to said plated through hole, the unetched metal pad further comprising a top surface, the unetched metal pad bottom surface and unetched metal pad top surface having a common pad width approximately equal to the through hole diameter.

Claims 10-14, 23, 24, 26 and 27. Claims 10-14, 23, 24, 26 and 27 are rejected under 35 USC § 103(a) as being unpatentable over Reed (U.S. Patent No. 4,964,948) in view of Reimann (U.S. Patent No. 4,663,497).

Claims 12-14 have been cancelled. New claims 28-31 comprehend subject matter present in the canceled claims 12-14.

The examiner concedes that Reed does not teach an aspect ratio greater than about 0.5, as claimed by amended claim 10, however, and the examiner asserts that Reimann teaches this limitation through his Figure 13 illustration. Applicants contend that the examiner's position is unsupported, and that amended claim 10 is allowable over Reed in view of Reimann.

First, Reimann provides no scale for his elements illustrated in Figure 13, nor does he indicate that any apparent spacing between his circuit lines is related to the size of the circuit

lines. 35 U.S.C. 113 provides that "[t]he applicant shall furnish a drawing where necessary for the understanding of the subject matter to be patented." And 37 CFR 1.83(a) provides that "[t]he drawing in a nonprovisional application must show every feature of the invention specified in the claims." A review of Reimann's Figure 13 reveals no scale, nor is any labeled spacing dimension indicated between the circuit lines 56. Reimann's claims do not teach the aspect ratio of amended claim 10. And where Reimann discusses Figure 13 (column 4, line 50, through column 5, line 10) he is silent upon the spacing dimensions and sizes of the circuit lines 56. Since patent illustrations are required only to show necessary elements, they may be stylized and are not required to be scale drawings nor accurately convey dimensions unless dimensions are necessary to the claims. There is **no presumption** that Reimann's Figure 13 accurately depicts the spacing scale or size of his circuit lines absent support within the specification, and there is no support here. Therefore, since the examiner's assertion that Reimann's Figure 13 teaches the aspect ratio claimed in amended claim 10, is unsupported by Figure 13, Reimann's specification, and Reimann's claims, it is not thought to be well taken.

Secondly, Reimann's circuit lines 56 are subtractively etched circuit lines (See Reimann at column 4, line 25, through column 5, line 10). As established above in the discussion of amended claim 9, subtractively etching circuit lines cannot produce the circuit line structure and line spacing claimed by amended claim 10. Therefore, amended claim 10 is believed allowable over Reed in view of Reimann.

The subject matter of new claim 28 is believed to be allowable over Reed view of Reimann for the same reasons established above; neither Reed nor Reed view of Reimann teach an *additively plated unetched metal pad* having a bottom surface plated directly onto the at least one plated through hole and thereby electrically connected to said plated through hole, the unetched metal pad further comprising a top surface, the unetched metal pad bottom surface and unetched metal pad top surface having a common pad width approximately equal to the through hole diameter.

Claims 11, 23, 24, 26, 27 are directly and indirectly dependent upon and include all of the limitations of amended claim 10, and are for the same reasons believed to be allowable over Reed view of Reimann.

Claims 29-31 are directly and indirectly dependent upon and include all of the limitations of claim 28, and are for the same reasons believed to be allowable over Reed view of Reimann.

Claims 15-20. Claims 15-20 are rejected under 35 USC § 103(a) as being unpatentable over Reed (U.S. Patent No. 4,964,948) in view of Reimann (U.S. Patent No. 4,663,497), and further in view of Kumagai et al. (U.S. Patent No. 4,942,079).

Claims 15, 17, 18 and 20 are all directly and indirectly dependent upon and include all of the limitations of amended claim 9. Claims 16 and 19 are directly and indirectly dependent upon and include all of the limitations of amended claim 10. The Kumagai et al reference is relied upon by the examiner to modify Reed in view of Reimann to teach a layer of dielectric material overlain the first circuitry of amended claim 9. Kumagai et al do not modify Reed in view of Reimann to teach all of the limitations claimed by amended claims 9 or 10. Therefore, for the reasons established above, claims 15-20 are believed to be allowable over Reed in view of Reimann and further in view of Kumagai et al.

In conclusion, the claims as amended and newly submitted are now believed to be in condition for allowance over the prior art of record.

Respectfully submitted,

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Enclosure